Design and Implementation of BSU for IFF Radar System using Xilinx Vertex2Pro FPGA

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Abstract

Beam steering unit (BSU) is one of the important subsystems of electronically scanned Antenna Array (ESAA) and is responsible for electronically steering the beam in a specified direction. The BSU receives the signals like beam pointing angle or sector scan and beam switching time from the signal processor of the IFF radar system over a serial RS-422 interface. Based on these input parameters it generates phase values for the phase shifters connected to the antenna elements. The switching of the beam from one position to the next depends on the switching time of the digital phase shifter.

In this paper the BSU has been designed and developed using state-of the art technology involving Xilinx Vertex2Pro based processor board and Phase shifter Interface Card (PIC). The Vertex 2Pro processor board receives the beam-pointing angle data on a serial RS-422 interface and then using serial controller passes this information to the processor to generate the required phase values for each of the 8 phase shifters. These phase values are sent to the phase shifters over differential line. The PIC converts the phase values from differential to TTL and laches it till next set of phase bits of phase shifter are received.

1. Introduction

Beam steering unit (BSU) is one of the important subsystems of the phased array radar [1]. It steers the beam electronically in a particular direction. Electronic scanning has various advantages over mechanical scanning as there is no need to rotate the antenna physically. The card has been designed and developed to steer the phased array antenna electronically. In this paper the BSU has been developed for electronically steering a planar antenna array for secondary surveillance radar commonly also known as IFF in military application. The BSU is designed for an 8x4 element planar antenna array. The radiating elements chosen for this phased array is printed dipole. This radiating element has been chosen because it has wide scan angle capability. The digital phase shifters used in this array are of 6-bits each. The scanning is carried out only in azimuth direction. Therefore total of 48 bits of the data is generated. It controls the beam pointing angle by issuing 48-bits digital phase information to 08-antenna elements of the phase array antenna; each element has 6-bit phase shifter. The BSU is composed of two modules – Vertex2Pro based processor board and Phase shifter Interface Card (PIC). Vertex2Pro based processor board receives BSU commands from Signal Processor and sends acknowledgement back and generates phase values for the phase shifters. The Phase shifter Interface Card (PIC) receives phase values on differential line and latched it till next update is received. The BSU calculates the phase values based on frequency of operation and the look angle. Two look-up tables angle-vs-48 bits phase values are generated. One is for transmission at a frequency of 1030Mhz and other is for reception at 1090MHz. Both the look-up tables are stored in SRAM of FPGA. The control logic, which is in FPGA, receives angle data from processor and selects appropriate phase values from the table and sends out over differential line to the Phase shifter Interface Card (PIC).

2. Design and development of BSU

BSU is designed and developed using state-of the art technology involving Xilinx Vertex2Pro based processor board and Phase shifter Interface Card (PIC) consisting of digital differential receivers and latches. The block diagram of the system is shown in Fig-1.

The interfacing between Vertex2Pro processor board and Phase shifter Interface Card (PIC) is through ±49 bits of discrete differential signals. These 49 bits consists of 48-bits of phase values and 01 bit to latch the phase values to the phase shifters. The IFF signal processor sends interrogation Mode signals to the processor board for selecting transmit beam phase values during transmission and receive beam phase values during reception for a particular look angle or sector scan mode. The processor board also receives the beam-pointing angle and beam switching time information on serial RS-422 interface and then using serial controller passes this information to the processor to generate the required phase values for each of the 8 phase shifters. The beam switching time depends on the switching speed of digital phase shifter. The digital

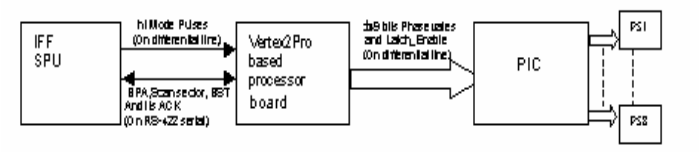


Fig-1: Block diagram of implementation of BSU

phase shifter used here has a switching speed of 2.5MHz.

3. Hardware design

3.1 Hardware design of Vertex2Processor board:

The Vertex2Pro FPGA (XCV30) is having two hardcore IBM Power PC and 30K logic cells for digital logic inside the FPGA. A Vertex2Pro FPGA allows making the design more adaptable to change and help in minimizing the hardware. It also facilitates the simplification of the debugging procedure. These features reduce the design and implementation cycle. The hardware design of the Vertex2Pro FPGA (XCV2P30) based board is given in Fig-2. The block diagram inside the FPGA is shown in Fig-3, The custom logic is having the look-up table with control logic.

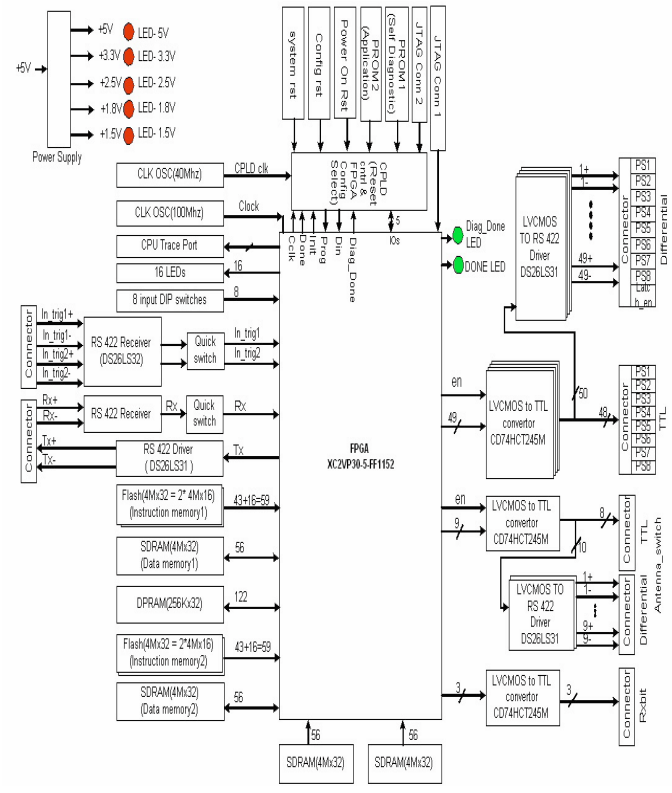


Fig-2: Block diagram of hardware design of BSU

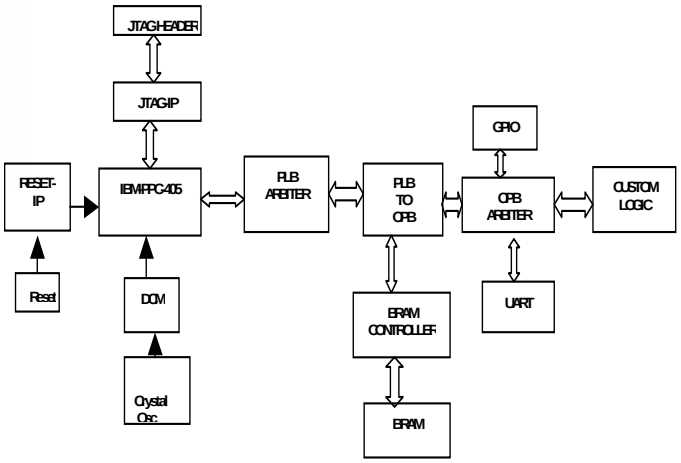


Fig-3: Block diagram of the modules inside the FPGA

Fig-4: Photograph of the BSU board

On power ON the board runs self-diagnostic test, if the tests passes then only hardware and software of user application is down loaded into the FPGA. The control logic of this is implemented in CPLD. The 49 bits of the data are sent out to PIC through differential line. The differential drivers are disabled after sending the phase values and enabled in next updates. The Photograph of the processor board is shown in Fig-4

3.2 Hardware design of PIC:

The phase shifters are mounted on the PIC card. This card receives ±48 bits phase value & one latch enable signals on discrete differential lines. The latch enable, enables the latches, which latches all phase values to the phase shifters. The card also provides power supply for the phase shifters. The hardware design of PIC is given in Fig-5. The photographs of front and back view of PIC card are shown in Fig-6 and Fig-7 respectively.

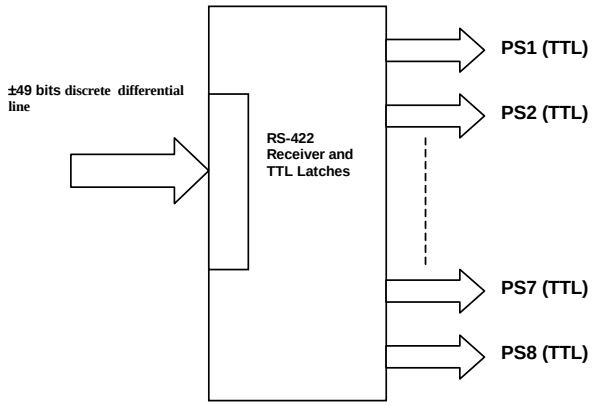


Fig-5: Hardware design of PIC

Fig-6: Front view of PIC card

Fig-7: Back view of PIC card

4. Software design

Software development: Following software modules have been developed towards BSU design and development.

4.1 Look-up table generation: Angles versus phase values (in bits) look-up table has been generated for angle between -60^0 and $+60^0$. The table has been generated using MATLAB.
The flow chart for calculating phase values for the phase shifters is shown in Fig-8

4.2 Application software development: Application software has been developed around IBM PPC 405 (Vetrex2Pro-FPGA). The flow chart of application software is shown in Fig-9.

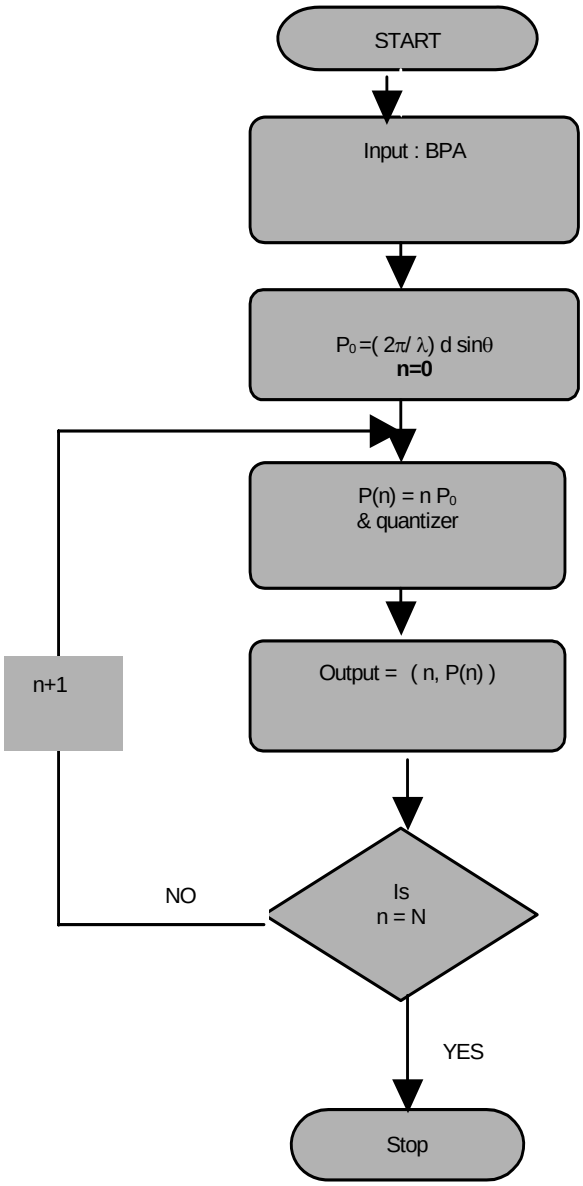


Fig-8: Flow chart for generating phase values

Integration and testing of BSU:
For testing the BSU a Graphical User Interface has been developed on PC. Following software has been developed towards this:

(a) Graphical User Interface (GUI)
(b) Software for RS-232 communication
(c) Integration of GUI and serial communication software.

Through GUI beam pointing angle or sector scan range is given to BSU. The BSU generates the phase values for the phase shifter of planar array antenna. The IFF radar system has been tested and validated. It is first tested on oscilloscope & then by using this BSU card along with PC to steer the phased array antenna. The test set up is shown in Fig-10. Fig-11 shows actual test

set used for validating the IFF radar system at different look angle and sector scan.

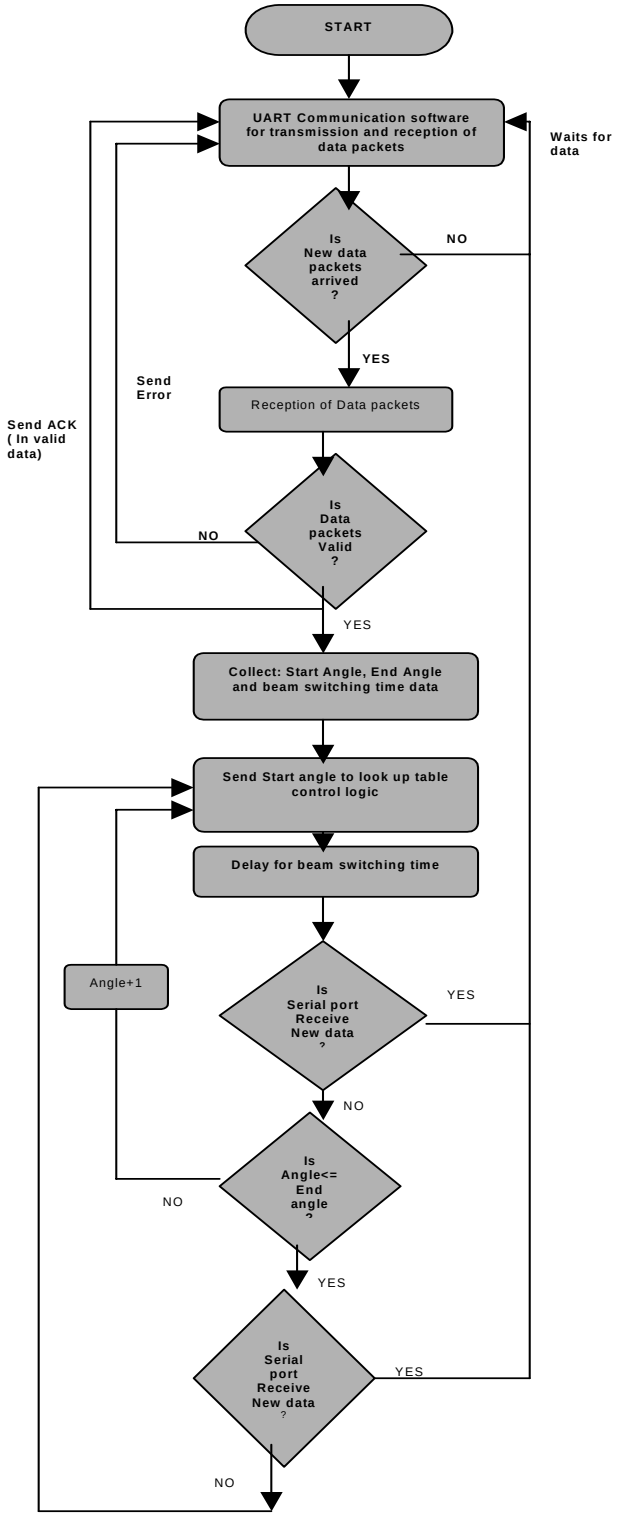


Fig-9: Flow chart for application software

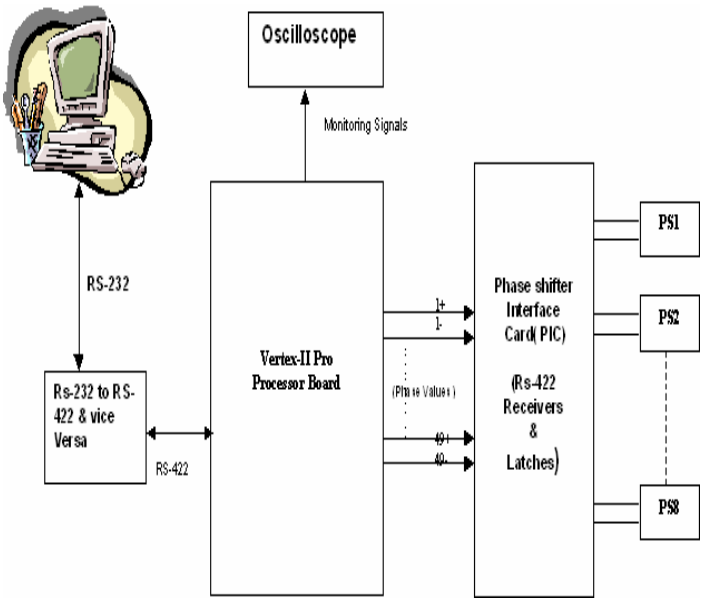
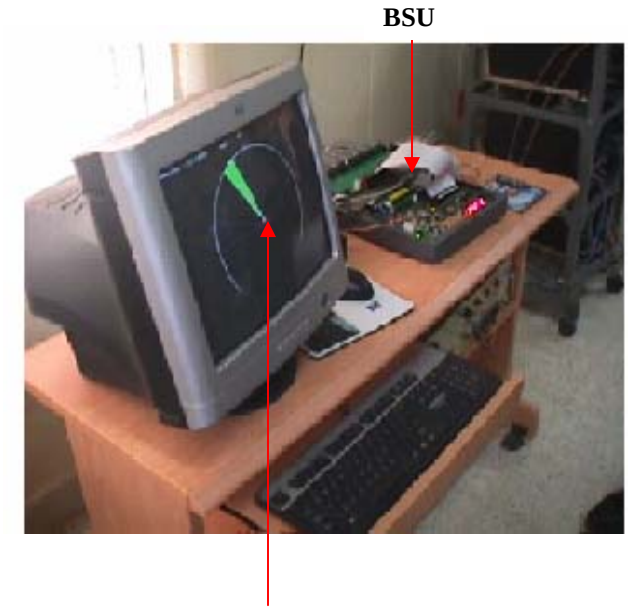


Fig-10: Test Set up to test the BSU



Display shows Antenna beam scanning. The scanning Angle is sent by the BSU to the PC for Display. The display also displays current beam width and scan angle.

Fig-11: Test Set up for testing actual IFF interrogator Radar system

Conclusion

The beam steering unit is realized by using of IBM PowerPC and FPGA (both are on single chip). The functional interface and timing requirements as per specification are achieved. This hardware is integrated and proven to show electronic scanning with phased array antenna for IFF interrogator system.

Acknowledgement

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