ANALYSIS OF DIGITAL MATCHED FILTER BASED ACQUISITION AND TRACKING SYSTEM FOR DIRECT SEQUENCE CDMA RECEIVER

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ABSTRACT

Direct sequence spread spectrum is the technique used in today’s most powerful cellular communications technology, code division multiple access. The most important aspect in the CDMA receiver is PN sequence synchronization. The digital matched filter (DMF) is a most powerful device that maximizes the synchronization system’s performance. This paper describes the design and performance analysis of the synchronization system that integrates the DMF in acquisition and delay locked loop (DLL) in tracking PN sequence. Simulation results have been obtained using Modelsim and Matlab.

1. INTRODUCTION

The basic concept of DS can be seen in Figure 1, where the data symbols to be transmitted are modulo-two added with the PN sequence at the transmitting end. The desired receiver has an exact replica of the transmitter’s PN sequence, and if it is able to align the PN code correctly, a second modulo-two addition with the PN sequence will lead to the recovery of the data symbols.

![Figure 1. The basis of DS spreading with XOR operations.](image)

DS spread spectrum systems have many other attractive features other than interference rejection. These include security, which was the reason for their invention. This stems from the fact that to an unwanted listener (preferably without knowledge of the spreading code) the transmitted signal is hard to differentiate from noise. Also, it has been shown that higher data rates and higher user capacity are possible with DS-based systems. For that reason CDMA has been steadily gaining popularity over its competitor, GSM (Global System for Mobile Communication).

2. PN SYNCHRONIZATION

The most sensitive aspect of a DS system is the synchronization of the transmitter's PN sequence to that of the receiver. This can easily be inferred from Figure 1, where an offset of even one PN chip can result in noise rather than a despread symbol sequence. Synchronization is composed of two elements: namely acquisition and tracking. These can be viewed as the alignment of the PN sequences, and the maintenance of this aligned state.

Synchronization systems use correlators to determine the correlation of the received signal to the local replica of the transmitted PN sequence. When a high correlation value is detected, acquisition has been achieved. As indicated on Figure 2, the point at which this decision is made (A) depends on a predetermined threshold value.

If no tracking system were present, the receiver would sample the correlation value at symbol intervals of point A on Figure 2. However, channel delay can cause the correlation value to drop below the threshold at these sampling instances, and cause the system to fall out of acquisition. A tracking loop modifies the sample timing so that sampling of
the correlation value occurs at the waveform’s peak (B).

![Figure 2 Correlation of received signal to PN](image)

Parallel correlator architectures are based on matched filters. These devices are based on an FIR structure with the PN sequence serving as the filter tap coefficients. As the received spread chip sequence slides through the input buffer, the chip-by-chip multiplications are done in parallel. Thus it takes at most one symbol duration $T$ to achieve acquisition.

### 3. Digital Matched Filter

This finite impulse response structure convolves the tap coefficient sequence $c(n)$, with the spread received sequence $r(n)$. As the $r(n)$ sequence slides through the tapped delay line, the asynchronous multiply and accumulate process calculates the correlation value. Thus a new correlation value is calculated at each chip interval. The polarity of the correlation peak, determines the polarity of the despread data symbol.

#### 3.1. DMF Implementation in Verilog HDL

The ideal matched filter considers an input stream of $\pm 1$. In the digital implementation of this system, the input sequence is a stream of zeros and ones. Thus the proposed design uses XOR operations in the place of multiplications. Further, as illustrated by Figure 3, the accumulate process is altered so as to reproduce the bipolar correlation output that would result if $\pm 1$ inputs were used.

The symbol-length PN code used was a 16 bit random sequence generated by Matlab. Given a nominal data over-sampling rate of 16, a 256-tap DMF was needed. This was accomplished with the use of a 256-bit static register that holds over-sampled PN sequence, a 256 bit shift register to hold the data, 256 XOR gates, and a 256 bit parallel adder. The shift register used to shift in the input data could be reused in all of the DMF instantiations.

The output range of the 256-tap DMF is $\{-256, 256\}$. Large positive or negative correlation values signify the reception of a valid symbol. Thus it can be intuitively justified to state that if a random sequence uncorrelated with the PN sequence were input to the DMF, the correlation value would be around zero. Since the input is random, it is fair to guess that half of the 256 XOR operations would result in high outputs and the rest in low outputs. An equal number of zeros and ones result in a zero output according to the scheme of Figure 3.

### 4. DMF Based Acquisition System

The DMF serves as the critical element in the PN acquisition system shown in Figure 5, as it performs the crucial task of correlating the spread received sequence with the local replica of the PN sequence. The bipolar output of the DMF is squared to create a unipolar sequence with an increased range (from $\{-256, 256\}$ to $\{0, 65536\}$). This increased range helps the detector’s decision-making.

Many different thresholds were used in the experimentation. For example, to prove the functionality of the DMF, a threshold of $256 \times 256 = 65,536$ was used. When noise and channel delay were considered, this threshold was lowered to around 25,000.

Before acquiring the PN sequence, the threshold constantly compares the received signal to its threshold. Once this threshold
been met (acquisition has been achieved) the detector sends a signal to the tracking circuit to start the tracking process. From this point on, the threshold comparison is done at symbol intervals. This is where the numerically controlled oscillator (NCO) comes in. It pulses the detector at every symbol period so that the detector can do its threshold comparison and output the despread data if still in acquisition.

In this design, the NCO is modeled as a counter that counts at the chip rate up to its maximum value of 255. When this expires, it activates the detector. The period of the NCO can be altered by the tracking circuitry, which will be our next topic of discussion.

5. DLL BASED TRACKING SYSTEM

A time varying transmission channel can cause delays in the received DS spread spectrum signal. This in turn causes the previously acquired PN sequence to fall out of acquisition if no sampling time correction mechanism is used. This mechanism is the tracking circuitry.

The delay-locked loop (DLL), sometimes called the “early-late gate”, is a common device used for tracking in DS systems. As shown in Figure 5, it consists of two branches, each very much similar to the acquisition circuitry.

We can intuitively see that if the incoming signal is on time, the acquisition branch of Figure 5 will sample at the peak correlation value and the two DLL branches’ outputs will equal, causing no error. If however, the incoming signal is delayed, one of the two branches of the DLL will output a higher value than the other. The difference of the two outputs, known as the timing error, is averaged out by the loop filter to produce the dc value. The sign and magnitude of this dc value then determines how much the phase of the NCO must be corrected to eliminate the timing error.

5.1. Loop Filter

The timing error sometimes exhibits erroneous jitter that can mislead the NCO’s timing circuitry. The FIR filter shown in Figure 4, is used to average out the timing error, e(n), so that a more accurate delay measurements, z(n), reaches the NCO.

\[ z(n) = e(n)h(0) + e(n-1)h(1) \]  

The loop filter used in this project was designed to be a compromise between practicality and performance. The ease of design of this filter in Verilog is worth mentioning. Since tap coefficients are sub-multiples of 2 (1/2 and 1/2), the two multiplications can be replaced by shifting. That reduces the filtering operation down to one major task, addition.

6. OVERALL SYSTEM

The overall system diagram is shown in Figure 5.

This system is based on a single user, dual-phase system such as binary phase shift keying (BPSK). In CDMA, RAKE receivers are used for synchronization of quad-phase signals using quadrature phase shift keying (QPSK) modulation. These receivers vary in complexity with increasing number of branches or “fingers.” A basic RAKE finger is usually very much similar to the system designed in this project. To take advantage of multi-path effects in a white-Gaussian noisy channel, each finger is separated from the next by a delay element. The outputs of all individual fingers are given weights, and then summed up to produce an output signal with maximum SNR.
7. SIMULATION RESULTS

In this section, we provide simulation results to verify our designs discussed in the above sections. We not only implemented the whole code synchronization system using Verilog hardware description language, but also implemented it using Matlab in order to verify our hardware design.

We start with addressing the digital matched filter simulation and then present Modelsim simulation results for the delay-locked loop circuit as well as the Matlab simulation results. Analytical comparisons between software and hardware simulation results are also provided. Finally, we present the S-curve performance of the DLL circuits and noise performance of the whole system.

All results given in this section are for a DS-CDMA system with a randomly generated PN code of length 16 chips. In order to focus on the code synchronization function, we only considered the single user BPSK scenario and ignored any multi-path or other channel fading. The received signal was spread with a processing gain of 16 and over-sampled by a factor of 16.

7.1. DMF Performance

First, the performance of the DMF design was verified via Modelsim and Matlab simulation. Altogether 10 symbols were used with a spreading factor of 16 and over-sampling rate of 16. The actual symbols we received are \[1, -1, 1, 1, -1, 1, -1, 1, -1\]. We can see that the positive and negative peaks of the matched filter output exactly represent the actually received symbols, which verified our DMF design.

7.2. Performance of DLL

The DLL is the heart of the tracking circuitry. The following simulation results show that our design of DLL works well. Figure 7 shows the instance when acquisition was obtained at time 5.38us and the ACQ signal went high; detector outputted \(S_0 = 0, S_1 = 1\), indicating a symbol “1” was received.

![Figure 6. Simulation result of the DMF in Matlab](image1)

![Figure 7. First Instance of Acquisition](image2)

![Figure 8. DLL locks when early and late branches output same correlation value.](image3)
In Figure 8, we can see that the DLL “locks” on to the incoming PN sequence, and from this point on, sampling occurs at the peak correlation value of 10000 (65,536). Also notice the bottom two signals in Figure 8, FilterIn and FilterOut, respectively. The input and output to the loop filter at the point that the DLL locks, are both zero. The DLL lock time for this particular simulation was four symbol periods.

![Figure 9. S-curve derived from Matlab.](image)

Figure 9. S-curve derived from Matlab.

The S-curve is an important performance indicator for the DLL. It displays the maximum range of the DLL, and how much delay it can adjust. Figure 9 shows the S-curve of the Matlab simulated DLL circuits. When there exists positive delay (late), the DLL outputs a positive number; when there exists negative delay (early), the DLL outputs a negative number.

Once the delay surpasses a certain limit, and the DLL cannot keep up, acquisition may be lost. When acquisition is lost during the tracking process, the entire acquisition process is restarted.

8. CONCLUSION

We implemented the DS/CDMA code for synchronization system including the matched filter, detector, loop filter, DLL, and NCO. The whole system was implemented in both Verilog and Matlab. The overall system of Figure 5 worked beautifully in both the Matlab and Modelsim implementation. The acquisition system successfully acquired the PN sequence and recovered the data symbols, and the DLL adjusted for delay and tracked the incoming PN code. Figure 10 displays a simulation window of the Modelsim simulator showing the recovered symbols.

![Figure 10. System Simulation in Modelsim.](image)

Figure 10. System Simulation in Modelsim.

Thus the DLL works well, adjusting the delay one chip per symbol period. Experimentation with quantizers at the output of the loop filter lead to lock times of one symbol period for some specialized cases.

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9. REFERENCES


