QUANTUM-DOT CELLULAR AUTOMATA OF FLIP-FLOPS

Anoop Vetteth, Konrad Walus, Vassil S. Dimitrov, Graham A. Jullien

ATIPS Laboratory
2500 University Drive, N.W., Calgary, Alberta, Canada, T2N 1N4
PH: 403-220-5806 Fax: 403-282-6855
e-mail: avetteth@atips.ca, walus@atips.ca. dimitrov@atips.ca, jullien@atips.ca

ABSTRACT

The use of quantum-dots is a promising emerging technology for implementing digital systems at the nano-scale level. Recently studied computational paradigms for quantum-dot technology include the use of locally connected quantum-dot cellular automata (QCA). This technique is based on the interaction of electrons within quantum dots that take advantage of quantum phenomena; the same phenomena that may prove problematic in future integrated circuit technologies as feature sizes continue to decrease. This paper proposes layouts for all the flip-flops. The potential application in telecommunications technologies of QCA and the proposed devices is widespread and clear. By taking full advantage of the unique features of this technology, we are able to create complete circuits on a single layer of QCA. Such devices are expected to function with ultra low power consumption and very high operating speeds.

1. INTRODUCTION

A QCA cell is a structure comprised of four quantum-dots arranged in a square pattern as shown in Figure 1.

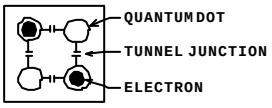

Figure 1. QCA cell

The quantum-dots within the cell provide 3D electron confinement and are capable of confining a controllable number of electrons. If the cell is charged with two excess electrons, they will tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. These electrons are able to tunnel between dots if the potential barrier that separates the dots is low. Provided that the electrons will always tend to occupy antipodal sites, there are two possible configurations, which can be used to encode binary information as shown in Figure 2.

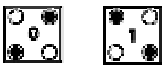

Figure 2. Binary encoding

Arrays of interacting QCA cells have been shown capable of all the logic functions required for universal digital design[1]. QCA architectures have been proposed with potential barriers between the dots that can be controlled and used to clock QCA circuits.

To date, experiments have been performed using QCA cells created from four aluminum metal islands connected via tunnel junctions made of Al/AlO_x[4-5]. Although these techniques have been used to verify the QCA concept, they suffer in that they require operating temperatures as low as 15mK. The operating temperature of QCA cells is highly dependent on the overall size of the quantum-dots. As the size of the dots shrink, the operating temperature of the cell rises. This is a result of the dependence of charging energy on dot size. To avoid problems associated with thermal fluctuations, the devices must be in an environment where the quantum-dot charging energy is much higher than the thermal energy i.e. $E_{charge} >> kT$. As nano fabrication technologies advance, the operating temperatures will rise. It is predicted that the

operating temperature of QCA cells with dots that are 2nm will be above room temperature, eliminating the need for refrigeration systems[7]. Switching in QCA is accomplished by switching the occupancy of the two electrons. Signals are carried down the arrays of QCA cells as a result of the interaction of adjacent cells. The topology of the QCA layout determines the interaction of the cells and hence the functionality of the overall circuit. The power consumption of QCA is low since only two electrons are moving[2-3]. Most of the power required by QCA circuits will be used by the clocking scheme.

1.1. QCA Clocking

The clocking of QCA can be accomplished by controlling the potential barriers between adjacent quantum-dots. When the potential is low the electron wave functions become delocalized resulting in no definite cell polarization. Raising the potential barrier decreases the tunneling rate, and thus, the electrons begin to localize. As the electrons localize, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cells act as virtual inputs and as a result, the actual inputs can start to feed in new values. This enables easy pipelining of QCA circuits. It has been shown that four clocking zones each pi/2 degrees out of phase is all that is required by any QCA circuit as shown in Figure 3.

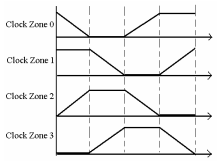

Figure 3. QCA clocking zones

These clocking zones provide a means of controlling signal propagation. This control is accomplished by attaching cells to clocking zones in such a way that they latch in succession in the direction of desired signal flow. The different clocking zones are indicated in our layouts by the different shades of gray background of the cells as shown in Figure 4

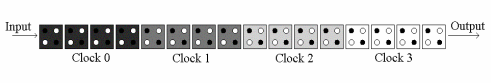

Figure 4. Different clocking zones..

1.2. QCA Logic

Adjacent QCA cells interact in an attempt to settle to a ground state determined by the current state of the inputs. This is most clear in the case of the QCA wire shown in Figure 5.

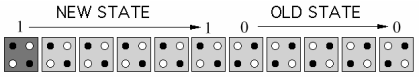

Figure 5 QCA wire

The polarization of the input cell is propagated down the wire, as a result of the system attempting to settle to a ground state. Any cells along the wire that are anti-polarized to the input would be at a higher energy level, and would soon settle to the correct ground state.

Computation with QCA is accomplished by designing QCA layouts, which exhibit the desired interaction of states. Consider the arrangements in Figure 6, demonstrating the QCA implementation of an inverter and a majority gate.

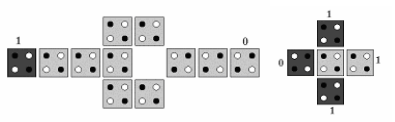

Figure 6. Inverter and majority gate

The ground state of the output cell of the above systems is a function of the shaded input cells and performs the desired logic function.

The majority gate is the fundamental QCA logic gate. The output cell will polarize to the majority polarization of the input cells. The Boolean expression for majority with inputs a, b and c is $m(a,b,c)=ab+bc+ca$. By fixing the polarization of any one of the inputs to the majority gate as logic 1 or logic 0, we obtain an OR gate or an

AND gate respectively. Other important logic layouts are described in reference [1].

1.3. QCA Design Rules

To ensure that QCA systems perform optimally there are some general design rules that should be followed while creating these systems. These design rules are based on the experience gained in creating and simulating the systems described later in this paper. They are as follows:

1. As a result of the non-linear cell-cell response function, which has a very high gain at the crossover point it has been found that cells tend to self re-enforce a weak input signal. It is wise then to ensure that at least two adjacent cells are present in any clocking zone to ensure this re-enforcing action takes place.
2. To ensure the proper result from the output of a majority gate, it is important that each of the signals arrives at the input at the same time and with the same signal strength. This can be easily accomplished by placing the cells that make up the majority gate in a separate clocking zone as its inputs as shown in Figure 7.

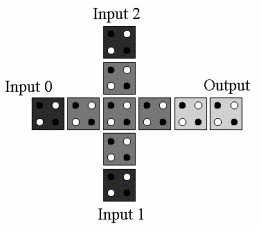

Figure 7 Clocking of majority gate

The three inputs to the gate are in one clocking zone. The majority gate itself is in the succeeding clocking zone. The output is taken off in yet another clocking zone.

3. Coplanar wire crossing is possible using a normal chain of QCA cells and an inversion chain of cells. This is possible because of the symmetry at the junction in which neither state of one wire with respect to the other is favorable, hence the ground states of the two wires are independent of each other. Imperfections in the layout of the system can lead to a breakdown in the symmetry of this system. To avoid the possibility of any switching interference while in the quantum analog state, the two lines are connected to different clocking zones.

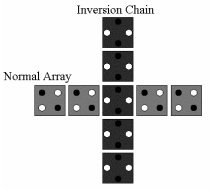

Figure 8 Clocking of co-planer wire crossing

2. FLIP-FLOP DESIGNS

In this section we describe the architectures for the four flip-flops. By replacing AND/OR logic with majority logic we are able to significantly minimize the total number of cells in the design. Since there is no static memory equivalent in QCA we have to create loops, which keep memory in motion. The proposed architectures of the flip-flops have been shown below.

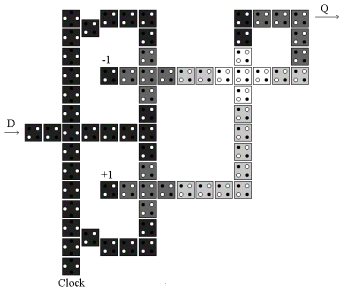

Figure 9 D Flip-Flop

The D flip-flop is constructed from 68 cells. Using one of the D-flip-flops in a random-access memory and assuming standard dimensions for each cell results in memory capacities on the order of $5\,G\text{-}bits/cm^2$. Designs for full random-access memories using QCA motion memories have been recently proposed [8]. The D flip-flop layout has been simulated using QCADesigner; a layout and simulation tool for QCA[6]. The simulation result for the D-flip-flop is shown below.

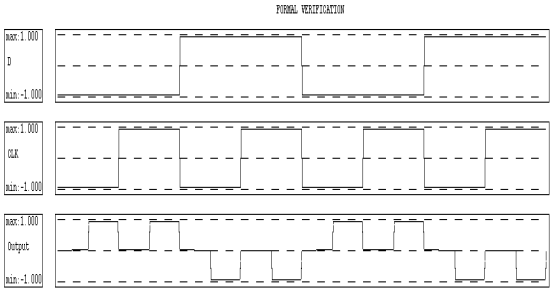

Figure 10 Simulation result for D-flip-flop

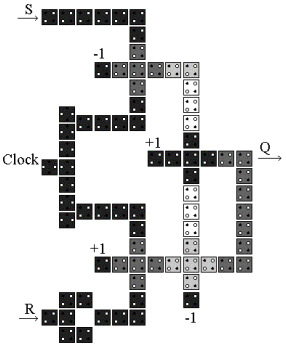

Figure 11 SR Flip-Flop

The SR flip-flop has 76 cells. The simulation result for the SR flip-flop is shown in Figure 12.

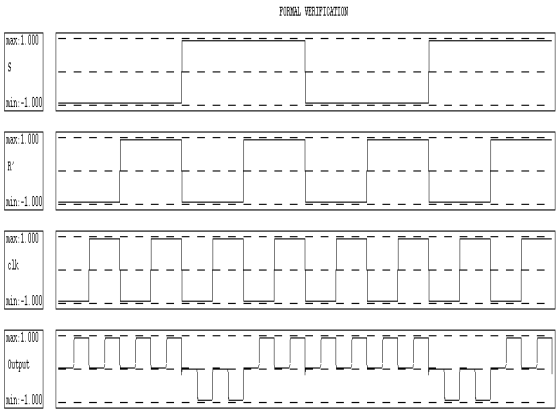

Figure 12 Simulation result for SR-flip-flop

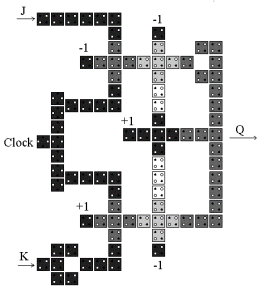

Figure 13 JK Flip-Flop

The JK flip-flop has 90 cells. The simulation result for the JK flip-flop is shown in Figure 14.

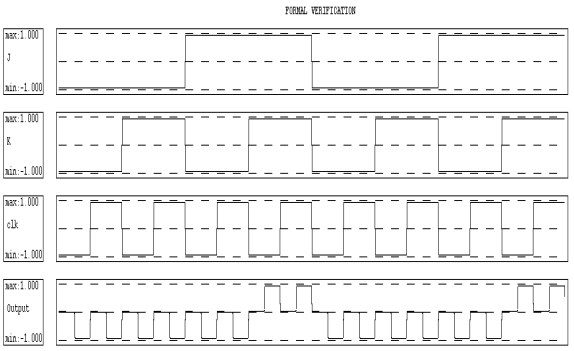

Figure 14 Simulation result for JK-flip-flop

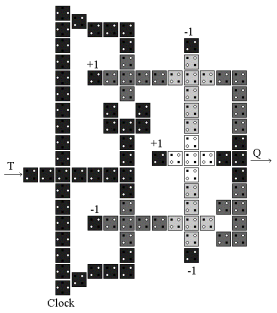

Figure 15 T Flip-Flop

The T flip-flop has 92 cells. The simulation result for the T flip-flop is shown in Figure 16.

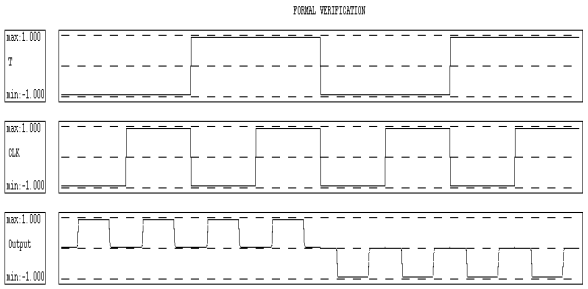

Figure 16 Simulation result for T-flip-flop

All the above flip-flops use one clocking cycle or four clocking zones.

3. CONCLUSIONS

In this work the authors have described the QCA computing paradigm and provided some detail into the current state of the technology. We have proposed layout of all the flip-flops based on this technology.

The proposed layouts are clearly significantly smaller than the same circuits using standard CMOS technology. The size reduction over standard CMOS is due to both the extremely small device size, as well as, the use of majority logic. The size measurements for both layouts are based on QCA cells, which are predicted to operate at room temperature. Using the unique features of QCA, we are able to layout all circuits on a single layer eliminating the requirement for complex interconnects found in CMOS.

All designs are carefully clocked using as simple a clocking layout as possible since clocking design rules have yet to be determined.

4. REFERENCES

[1] Tougaw, P.D., Lent, C.S., "Logical devices implemented using quantum cellular automata", *J. Appl. Phys.*, American Institute of Physics, **75** (3) 1818, 1994

[2] Tougaw, P.D., Lent, C.S., "Dynamic behavior of quantum cellular automata", *J. Appl. Phys.*, American Institute of Physics, **80** (8) 4722, 1996

[3] Timler, J., Lent, C.S., "Power gain and dissipation in quantum-dot cellular automata", J. Appl. Phys., American Institute of Physics, **91** (2) 823, 2002

[4] Islamshah, A., Orlov, A.O., Kummamuru, R.K., Bernstein, G.H., Lent, C.S., Snider, G.L., "Experimental demonstration of a leadless quantum-dot cellular automata cell", *Appl. Phys. Lett.*, American Institute of Physics, **77** (5) 738, 2000

[5] Orlov, A.O., Amlani, I., Toth, G., Lent, C.S., Bernstein, G.H., Snider, G.L., "Experimental demonstration of a binary wire for quantum-dot cellular automata", *Appl. Phys. Lett.*, American Institute of Physics, **74** (19) 2875, 1999

[6] Walus, K. "QCADesigner Homepage", http://www.atips.ca/~walus, *ATIPS Laboratory*, University of Calgary, Calgary, AB, 2002

[7] Porod, W. "Quantum-dot devices and quantum-dot cellular automata", *Inter. J. Bifurcation and Chaos*, World Scientific Publishing Company, **7** (10) 2199, 1997

[8] A.Vetteth, K.Walus, G. A. Jullien, V.S. Dimitrov, "RAM Design Using Quantum-Dot Cellular Automata", 2003 Nanotechnology Conference and Trade Show.