MODIFIED DECT 3G PHYSICAL LAYER WITH IMPROVED MULTI–RATE CAPABILITY

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ABSTRACT

The DECT (Digital Enhanced Cordless Telecommunications) standard is a member of the IMT–2000 family. The 3rd Generation (3G) DECT physical layer provides multi–level modulation capability for bit–rates going upto 3.5 Mbps. Recently, a Wireless Local Area Network (WLAN) has also been proposed based on the DECT standard [1]. However, DECT is inefficient for providing low bit–rate channels (e.g., 8 kbps for voice) and does not have sufficient granularity in the bit–rates supported, unlike the 3G CDMA standards. We present a novel modification to the DECT physical layer for creating low bit–rate channels as well as for increasing the granularity. An important feature of the proposal is that the 3G DECT radio hardware needs no change – only the software in the radio is new. The new bit–rates are achieved by employing proportionately less bandwidth. The sensitivity too increases likewise. New transmitter and receiver algorithms are developed and issues regarding their implementation are discussed.

1. INTRODUCTION

1.1. Overview of DECT 3G physical layer

The 3G DECT standard is based on Multi–Carrier TDMA–TDD [2]. The carriers are spaced 1.728 MHz apart in the frequency band 1880–1937 MHz. The TDMA frame consists of 24 full time–slots every 10 ms, at a gross symbol rate of 1.152 Msymbols/sec. Each frame is divided into two halves of twelve contiguous slots, for the uplink and downlink directions respectively. Each full slot is of 480 symbols, with a 32–symbol S–field for synchronization, 64–symbol A–field for signaling, 328–symbol B–field for payload, and 56–symbol guard band. The 3G physical layer specifications [3] allow $\pi/4$–shifted DQPSK and $\pi/8$–shifted D8PSK modulation in addition to 2–level modulation, which can be either $\pi/2$–shifted DBPSK, or GFSK as in the 2G standard.

In addition to the full slots, DECT defines half slots and double slots, whose meaning is self–evident. However, as a result of the fixed overhead of the S– and A–fields and the guard symbols, the payload in the half–slot is only 25% of the full–slot payload, resulting in a high TDMA overhead–to–payload ratio. Conversely, the double slot has a payload that is 2.5 times that of the full slot. The range of bit–rates supported in the 3G standard, if various slot–sizes and modulation–levels are exploited, is 8–2880 kbps (from one half–slot and binary modulation, to 12 full slots and 8–level modulation). However, the granularity is coarse when the bandwidth–efficient 4– and 8–level modulation formats are employed, and as mentioned above, the TDMA efficiency is poor for low bit–rates.

1.2. Limitations of Low Bit-Rate Service in DECT

Today a host of services require low data rate channels, e.g. voice at 6–8 kbps, messaging, always–on upstream Internet access, etc. One way of creating such channels without the inefficiency associated with the use of half–slots, is to increase the frame duration. This, however, introduces undesired latency. Further, since the peak transmit power is fixed, the receiver sensitivity remains unchanged, even though one effectively employs proportionately less bandwidth due to the lower duty cycle. An alternative which does not reduce the bandwidth employed and does not increase latency, but improves the sensitivity, is the use of error control coding. For example Rate–1/4 codes can be used with 8 kbps payload in a full slot.

1.3. Use of Narrow–band Sub–Channels

A new scheme is proposed for supporting low bit–rate channels, which has proportionately higher receiver sensitivity (for the same peak transmit power) and employs lower bandwidth. In the new scheme, data is transmitted at a fourth of the present symbol rate of 1.152 MHz. Since the bandwidth requirement also comes down by the same factor, to 432 kHz, four sub–channels can be accommodated on one DECT carrier. The noise power in the receiver reduces by a fourth in the sub–channel relative to the full channel, resulting in proportionately higher sensitivity.

Before proceeding to discuss the new proposal in detail, we briefly look at the architecture of the 3G DECT transceiver.

2. OVERVIEW OF EXISTING 3G TRANSCEIVER

A conventional 3G transceiver employs a double conversion architecture with two Intermediate Frequencies (IF) in the receiver and a single IF in the transmitter. More recent designs based on a so–called zero–IF receiver have been implemented for some standards. A conventional transceiver has been implemented recently for DECT [4].

2.1. Transmitter

The 3G DECT transmitter consists of a baseband section, IF section and RF front end. The baseband I and Q signals are generated using a RAM or ROM based look-up table and a dual–DAC combination, with each DAC being updated six times in each symbol duration. The baseband pulse in DECT has root–raised cosine spectrum with symbol duration $T_s = (1/1.152)\ \mu s$ and excess bandwidth factor of 0.5. In the implementation, the RRC pulse is truncated to three symbols, without violating the spectral mask [3]. Based on the particular pattern of neighboring symbols (ISI), different sets of six samples corresponding to the symbol being transmitted are read from the RAM, and fed to the DACs. The I and Q signals thus generated are then fed to a balanced I–Q modulator, which outputs the signal at an IF of 131.328 MHz. The IF signal is then translated to the appropriate carrier in the DECT band.

2.2. Receiver

The 3G DECT receiver [4] consists of a LNA, the first mixer–downconverter, an IF channel selection filter, followed by a second mixer–downconverter, and a linear AGC stage. Since the transceiver operates in TDD mode, many of the components are shared with the transmitter. The output of the AGC stage is sampled using an ADC and the samples are then processed in a DSP. The second IF is chosen to be equal to $(n+0.5)$ times the bandwidth (n being an integer), so that the bandpass signal can be sampled at a sampling rate equal to twice its bandwidth without aliasing. Thus, with the bandwidth being 1.728 MHz, the sampling rate $(= 1/T)$ is 3.456 Msamples/sec for a second IF equal to 9.504 MHz (obtained with $n = 5$). The IF of the sampled signal is aliased to 864 kHz (or $\pi/2$ in the discrete–time world) nominally. Since the symbol rate $(= 1/T_s = 1/3T)$ is equal to 1.152 Msymbols/sec, we get three samples per symbol duration. The samples are fed to a DSP, which perform the tasks of demodulation, acquisition, synchronization, frequency offset and phase estimation and data detection [4].

3. TRANSCEIVER FOR A NARROW–BAND SUB–CHANNEL

3.1. Transmitter

Four sub–channels are multiplexed in 1.728 MHz. These sub–channels could be generated at different transmitters in the uplink (Subscriber terminal to Base–station) direction. Depending on the tolerance of the crystal oscillators, the excess bandwidth of the RRC pulse may need to be reduced a little below 50% to create a guard band. The symbol rate in each sub–channel is $1.152/4 = 288$ kHz. Each sub–channel occupies $1.728/4 = 432$ kHz, with center frequencies $f_k = -864 + 216(2k+1)$ kHz for $k = 0, 1, 2, 3$.

3.1.1. Transmitter Algorithm

The same RAM–DAC circuitry used for generating the full 864 kHz baseband signal can be used for generating the sub–channel signals, by implementing Single Side Band (SSB) modulation. The baseband signal in the k^{th} sub–channel is given by

$$\tilde{s}_k(t) = I_k(t) + jQ_k(t)$$

where $I_k(t)$ and $Q_k(t)$ are the in–phase (I) and quadrature (Q) signals given by

$$I_k(t) + jQ_k(t) = \sum_p (I_{kp} + jQ_{kp}) .g(t - pT_s) \quad (1)$$

The modulated SSB signal in the k^{th} sub–channel with center frequency f_k can be expressed as

$$m_k(t) = \tilde{s}_k(t).e^{j2\pi f_k t} \quad (2)$$

where in–phase and quadrature components $m_{kr}(t)$ and $m_{ki}(t)$ respectively are a Hilbert transform pair:

$$\begin{gathered} m_{kr}(t) = I_k(t).cos(2\pi f_k t) - Q_k(t).sin(2\pi f_k t), \\ m_{ki}(t) = Q_k(t).cos(2\pi f_k t) + I_k(t).sin(2\pi f_k t), \\ with, m_{ki}(t) = \hat{m}_{kr}(t) \end{gathered} \quad (3)$$

The modulated signal is

$$\begin{aligned} m_{IF,k}(t) &= Re\left[m_k(t).e^{j2\pi f_{IF} t}\right] \\ &= Re\left[\tilde{s}_k(t).e^{j2\pi(f_{IF}+f_k)t}\right] \quad (4) \end{aligned}$$

Finally the transmitted signal in any DECT channel is the sum of four frequency–multiplexed sub–channels:

$$\begin{aligned} m_{IF}(t) &= \sum_{k=0}^{3} m_{IF,k}(t) \\ &= Re\left[\sum_{k=0}^{3} \tilde{s}_k(t).e^{j2\pi(f_{IF}+f_k)t}\right] \end{aligned}$$

It is clear that sub–channels with positive f_k are transmitted with upper side band, and those with negative f_k with lower side band as shown in Figure 1.

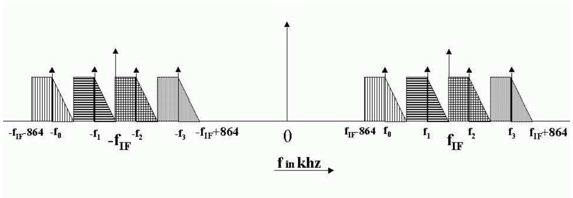

Figure 1: *Spectrum of four sub–channels at IF*

3.1.2. Implementation issues in Transmitter

The number of different sample sets to be stored in RAM depends on the length of RRC pulse and the number of possible amplitude levels for I and Q. In case of $\pi/4$–DQPSK, I(and Q) is either from $\{0, \pm 1\}$ or $\{\pm 1/\sqrt{2}\}$ in alternate symbol periods. Now for a three–symbol RRC pulse, when the middle symbol $\in \{\pm 1/\sqrt{2}\}$, the number of possible combinations is 18, and when the middle symbol $\in \{0, \pm 1\}$, it is 12. Thus, for the full–band channel $\pi/4$–DQPSK (1.728 MHz), a total of 30 sets of 6 samples (refer section 2.1) each need to be stored in RAM. The memory required is thus 30*6=180 words. For $\pi/8$–D8PSK, a total of 180 such sets need to be stored and the memory required in this case is 180*6= 1080 words.

For the narrow–band sub–channel scheme, the number of samples/symbol increases by 4, and the number of sub–channel frequencies is 4. Thus the memory size increases by 16, i.e., it is about 3 kwords for $\pi/4$–DQPSK and 17 kwords for $\pi/8$–D8PSK. These are still fairly small at current technology levels. The memory requirement can however be reduced if signal symmetry (e.g., signal sets which differ in sign only) is exploited.

3.2. Receiver

In order to detect the data in any one sub–channel, the remaining sub–channel signals must be filtered out. This can be combined with the matched filtering for the desired channel, as discussed below.

3.2.1. Receiver Algorithm

The received IF signal in the absence of noise is

$$r(t) = Re\left[\sum_{k=0}^{3} \tilde{s}_k(t).e^{\jmath 2\pi(f_{IF}+f_k)t+j\theta_k}\right]$$

where θ_k is the phase of k^{th} subcarrier at the receiver. The complex baseband equivalent of the above received signal can be expressed as

$$\tilde{r}(t) = \sum_{k=0}^{3} \tilde{s}_k(t).e^{\jmath 2\pi f_k t+j\theta_k}$$

With the baseband bandwidth of 864 kHz, the minimum sampling rate ($1/T$) required is 1.728 Msamples/sec. Since the symbol rate ($1/T_s = 1/6T$) is $1.152/4 = 288$ ksymbols/sec, we get 6 samples per symbol duration. The samples of $\tilde{r}(t)$ for $f_k = -864 + 216(1+2k)$ at $t = nT$ are

$$\begin{aligned} \tilde{r}[n] &= \sum_{k=0}^{3} \tilde{s}_k[n].e^{\jmath(2k-3)n\pi/4+j\theta_k}, where \\ \tilde{s_k}[n] &= \sum_p (I_{kp} + j.Q_{kp}).g(n-6p) \end{aligned}$$

The matched filter for sub-channel i is

$$g_i[n] = h_i^*[-n] = g[n].e^{\jmath(2i-3)n\pi/4}$$

The filter output is given by

$$\begin{aligned} y_i[n] &= g_i[n] \otimes \tilde{r}[n] \\ &= \sum_{m=n-N+1}^{n} \tilde{r}[m]g_i[n-m] \end{aligned} \tag{5}$$

where $g_i(n)$ is assumed be of length N.
Let us now consider the demodulated filter output:

$$\begin{aligned} x_i[n] = y_i[n].e^{-\jmath(2i-3)n\pi/4} \\ = \textstyle\sum_{m=n-N+1}^{n} \left(\tilde{r}[m]g[n-m].e^{\jmath(3m\pi/4)}\right).e^{-\jmath 2im\pi/4} \end{aligned} \tag{6}$$

Since $g_i[n]$ is bandlimited to $(2i-4)\pi/4$ to $(2i-2)\pi/4$, only the i^{th} sub-channel signal will remain after filtering:

$$x_i[n] = \sum_p (I_{ip} + jQ_{ip}).f(n-6p).e^{j\theta_i} \tag{7}$$

where $f(n-6p) = \sum_{m=n-N+1}^{n} .g[m-6p].g[n-m]$ is a raised cosine pulse sampled at six times the symbol rate. Therefore

$$f(6k) = \left\{ \begin{array}{l} 1,\ k=0 \\ 0,\ elsewhere \end{array} \right\} \tag{8}$$

Equation (7) can be simplified as

$$x_i[n] = \sum_p (I_{ip} + jQ_{ip}).f(n-6p).e^{j\theta_i} \tag{9}$$

It is clear that

$$x_i[6k] = (I_{ik} + jQ_{ik}).e^{j\theta_i} \tag{10}$$

Thus, the symbols of the i^{th} sub–channel can be obtained after the carrier phase is compensated for. If θ_i changes slowly due to an unavoidable residual frequency offset, it can be tracked as in [5]. Note, in (6) that we have a 4–point DFT of a sequence, if it is assumed without loss of generality that N is divisble by 4. The sequence whose DFT is to be found need be computed only once for each n.

3.2.2. Implementation issues in Receiver

It is shown in [4] that in–phase and quadrature components of $\tilde{r}(n)$ can be obtained from $r(n)$ without computation, and at a sampling rate of 1.728 MHz each, by performing trivial operations (multiplying by $(-1)^n$) on alternate samples of $r(n)$. However, the samples of the in–phase and quadrature components thus obtained are offset in time with respect to each other by a half sample–duration (at 1.728 MHz). This would not have mattered if these components were to be individually filtered by the RRC sequence, as suitably half–sample offset RRC sequences can be employed for the in–phase and quadrature components respectively. In Equation (6), however, $\tilde{r}(n)$ has to be twiddled by a complex exponential sequence before filtering with the RRC sequence. Hence, we must necessarily have the in–phase and quadrature signals sampled at the same time instant. Thus, one of the two sequences obtained as described above must be re-sampled using a half–sample delay [6]. Complexity–wise, this is equivalent to computing the Hilbert Transform of $r(n)$ to obtain the in–phase and quadrature sequences.

A practical issue is the resolution needed in the ADC. When the ADC is sampling a full–band channel, the resolution needed is around 5 bits – so that the quantization noise is negligible compared to the input thermal noise. However, when the narrow–band sub–channels are present, and different sub–channels are received with different power levels, the resolution needed is higher. If the resolution of the samples of the desired sub–channel is of the order of 5 bits as before, the ADC resolution required depends on the level of adjacent channel interference (ACI) the receiver is expected to tolerate. For example, if 18 dB ACI is to be tolerated for the sub–channels put together, the ADC must have at least 8–bit resolution.

Thus, we see that the ADC resolution increases unless power control is introduced for the sub–channels. This is not impractical today – low cost PAs with power control are widely available, and the desired transmit power level can be easily estimated in a TDD system from the received power level.

4. CONCLUSIONS

A novel scheme is proposed for supporting low bit–rate services in DECT with low bandwidth utilisation and improved receiver sensitivity. This scheme, which employs narrow–band sub–channels of the DECT channel, does not require a new trans–ceiver chipset to be developed. Only the transceiver DSP software needs to be changed. The algorithms needed to implement the new scheme have been shown to be simple, requiring only FIR filtering and DFT computations.

By employing one or more narrow–band channels, and full/double/multiple slots, finer granularity in bit–rates is achievable even when multi–level modulation is employed. This will mean more system capacity by accomodating a richer variety of services. Further, when employing multiple sub–channels from a single subscriber terminal in the uplink direction in order to provide a higher bit–rates service, one can have the sub–channels in the same time–slot or in different time slots. For a given transmit power level, this allows the energy per bit to be varied, which in turn permits the link margin to be varied as needed.

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