ABSTRACT

The DECT (Digital Enhanced Cordless Telecommunications) standard is a member of the IMT-2000 family and the third Generation 3G DECT physical layer provides multi-level modulation capability enabling 2 Mbps services. In this paper, we present a 3G DECT receiver that can handle channels with delay spread. This receiver is based on a coherent I-Q demodulator with a fractionally spaced equalizer. The soft digital FM demodulator present in the 3G receiver ensures backward compatibility with 2G DECT equipment. The soft digital FM demodulator, being non-coherent, is robust to frequency offset and multipath delay spread, because of capture effect, which can be used for slot acquisition and timing synchronization.

1. INTRODUCTION

1.1 Overview of 3G DECT Physical Layer

The Digital Enhanced cordless telephone (DECT) standard is highly suitable for providing wireless local loop with both voice and data services. While currently DECT supports a peak bit rate of 1.152 Mbps on 1.728 MHz, the 3G evolution of DECT can provide up to 3*1.152 = 3.456 Mbps to fixed users using the same bandwidth.

The 3G physical layer specifications [2] allow π/4-shifted DQPSK and π/8-shifted D8PSK modulation [6] in addition to 2-level modulation, which can be either π/2-shifted DBPSK or GFSK. In order to ensure backward compatibility, both the S-field used for synchronization, and the A-field containing control information, are always transmitted using 2-level modulation only. The π/2-shifted DBPSK modulation can be detected with a GFSK receiver and the new receiver should be capable of detecting GFSK modulation. The 3G receiver (that has been implemented at IITM) is a double-conversion receiver with the receive chain consisting of a LNA, the first mixer-downconverter, an IF channel selection filter, followed by a second mixer-downconverter, optional second IF filter, and a linear AGC stage.

The output of the AGC stage is sampled using an ADC and the samples are then processed in a DSP. The second IF is chosen to be equal to (n+0.5) times the bandwidth (n being an integer), so that the bandpass signal can be sampled at a sampling rate equal to twice the bandwidth of the signal without aliasing. Thus, with the bandwidth being 1.728 MHz, the sampling rate (=1/T) is 3.456 Msamples/sec for a second IF equal to 9.504 MHz (obtained with n=5). The IF of the sampled signal is aliased to 864 kHz (f_s) nominally. Since the symbol rate (=1/T_s=1/3T) is equal to 1.152 Msymbols/sec, we get three samples per symbol duration. The 3G receiver also employs a soft digital FM demodulator for backward compatibility.

The sensitivity of the 3G DECT I-Q demodulator must be –92 dBm while the 2G DECT FM demodulator must meet only –86 dBm sensitivity. However in the presence of

The 3G DECT Receiver for Frequency Selective Channels

G. Ramesh Kumar                         K.Giridhar
Telecommunications and Computer Networks (TeNeT) Group
Department of Electrical Engineering
Indian Institute of Technology, Madras
Chennai-600036 India.
ramesh_gani@yahoo.com          giri@tenet.res.in
frequency offset and multipath delay spread it is virtually impossible to reliably estimate slot boundary information using the I-Q coherent demodulator. Even though the sensitivity of the FM demodulator is 6 dB poorer than the I-Q demodulator (for BER of $10^{-3}$), the slot-boundary acquisition performance of the soft FM demodulator is good even at –92dBm.

2. RECEIVER DESIGN

We now discuss the major issues involved in designing the new receiver algorithm on the DSP as shown in the figure 1.

Figure 1. Block diagram for new 3G DECT receiver

2.1 Soft Digital FM Demodulator – Acquisition and Timing Synchronization

The soft digital FM demodulator present in the 3G receiver provides backward compatibility for demodulating GFSK modulated signals received from 2G equipment. Because of the bandpass sampling this is implemented in side the DSP [2]. In the new receiver, which can handle ISI channels the soft FM demodulator is used to perform the following in the new receiver

- Slot boundary acquisition on power-up, or whenever the frame or slot synchronization is lost.
- Detection of the start of the data field.
- Symbol clock phase recovery (with a resolution of $T_s/12$) in every slot

The digital FM demodulator is implemented using an inverse-tangent look-up table followed by a differentiator[3]. The baseband output of the FM demodulator is then fed to the acquisition and synchronization algorithm [5]. During the acquisition phase, the algorithm searches for the S-field preamble by correlating the demodulated data with a stored pattern. Once the preamble is found, demodulation is done to recover data and detects the presence of the synchronization pattern by doing digital correlation, to locate the exact start of the data field in the slot. Now symbol clock phase is obtained from the peak of correlation of the preamble pattern.

2.2 Clock and Carrier Synchronization

The DECT specifications permit a maximum clock frequency difference of 35 ppm (25 ppm at Portable Part and 10 ppm at Radio Fixed Part). Using a 27.648 MHz oscillator, the drift, $\Delta T$, in one slot duration (i.e., 480 symbols) as a fraction of the symbol duration $T_s$ is $\Delta T/T_s = 0.0168$. Since this is a very small fraction of the symbol duration, it is sufficient to recover the phase of the symbol clock at the beginning of each slot, and use it for the entire slot duration without tracking.

The DECT specifications allow a net variation of up to ±100 kHz at the demodulator. For a 100 kHz frequency offset, the phase deviation in one symbol duration would be $\Delta \Phi = 2\pi \cdot 100 \cdot 10^3 \cdot \left(1/1.152 \cdot 10^6\right) = 0.1736 \cdot \pi$ rad/symbol, which is larger than the smallest symbol-to-symbol shift in a $\pi/8$-D8PSK system. Hence, it is necessary to first estimate the received IF frequency with sufficient accuracy and ensure that any residual frequency offset merely contributes a small phase offset in each symbol. The
carrier frequency ($\delta f$) and initial phase ($\theta$) estimation is explained in detail in [4]. As shown in the figure2, the matched filtered samples are derotated with the estimated $\delta f$ and $\theta$. The residual phase drift is then tracked and corrected at the end of each symbol during data detection. The Doppler shift for portable applications is very small and DECT does not provide explicit fade margins for short-term fading.

2.3 Fractionally spaced Equalizer and Data Detection

Unlike GSM, DECT by itself does not specify any particular bit pattern for equalization. However, the preamble that is meant for detection of the start of the data field is used by us to train the equalizer coefficients. Prior to equalization, the location of the synchronization field is determined with the help of soft digital FM demodulated samples. Though the alternating bit pattern (preamble) is also known at the receiver, it is not suitable for equalizer training. The filter coefficients are not adapted with time as the accumulation of the clock error is very small compared to the symbol duration and also because we have a single tap tracker during data detection.

The equalizer is trained as shown in the figure2, with the known symbols of the synchronization field $d(n)$, using LMS method. The input, $x(n)$, to this fractionally spaced equalizer is at the rate of three samples per symbol duration, but the filter coefficients are updated only at symbol rate with error, $e(n)$, computed once every symbol duration using the LMS equation.

DFE is implemented instead of linear equalizer as DFE performs better than the later. Decision feedback equalizer is trained similar to the linear equalizer except that the input vector contains the feedback elements along with $x(n)$. DFE performs better than linear equalizer as the feedback elements nullify the ISI due to the previous symbols.

In simulations two feedback elements are taken and the convergence controller is chosen to be different for the feedback and feed forward elements to optimize the performance. After the equalizer is trained the entire data packet is convolved with the equalizer, which can be either linear equalizer or DFE.

Even after the frequency and phase offset compensation and equalization, the residual carrier frequency offset that can be treated as the slowly varying phase is tracked before detecting the bits. The procedure of data detection is differentially coherent. Thus symbols are detected in the data field of the slot by tracking the carrier phase offset and any other errors using an adaptive algorithm as shown in figure2.

After equalization the received complex baseband samples, at the correct sampling phase, $s(n)$, thus contain an $e^{i\delta \theta}$ term appearing as a multiplication factor, where $\delta \theta$ is the residual phase error because of the frequency offset error. In order to correct for the multiplicative term, these samples are first multiplied by a complex weight, $w(n-1)$, of unit magnitude before detecting the symbol. The complex weight, $w(n-1)$, is estimated recursively based on the Least Mean Squares (LMS) algorithm as shown in the figure.

3. SIMULATION RESULTS

Computer simulations were performed to study the BER performance curves and the error convergence curves for a few ISI channels. The training of the equalizer was
repeated twice with the known symbols of the synchronization pattern to get better performance.

BER curves shown in figures 3 and 4 are for two channels A and B respectively, which are defined in the table 1. Apart from ISI, frequency offset of 30KHz is also present. In each of these figures the BER curves for differentially coherent DBPSK (with and without frequency offset) are also shown. The convergence curves for both DFE and LE are shown in the figure 5.

<table>
<thead>
<tr>
<th>Channel</th>
<th>Delay</th>
<th>Gain</th>
</tr>
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<tbody>
<tr>
<td>A</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>.75T</td>
<td>.7</td>
</tr>
<tr>
<td></td>
<td>1.5T</td>
<td>.4</td>
</tr>
<tr>
<td>B</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>.5T</td>
<td>.5</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td>.2</td>
</tr>
</tbody>
</table>

Table 1. Different ISI patterns

Figure 3

Figure 4

Figure 5

4. CONCLUSIONS

A receiver design that can handle ISI channels for 3G DECT physical layer has been presented. Issues in carrier and clock synchronization to enable coherent detection have been discussed. The entire receiver algorithm with matched filtering, frequency offset estimation followed by equalization and tracking is simulated in MATLAB and found to be working. The entire algorithm is implemented on DSP platform and the integration of the receiver algorithm with the hardware platform is being carried out.
5. REFERENCES


6. Appendix

6.1 DECT Framing Overview

The 2G DECT standard is based on Multi-Carrier TDMA-TDD. There are ten carriers within the frequency band 1880-1900 MHz, each with a bandwidth of 1.728 MHz. The basic TDMA frame consists of 24 slots over 10 ms, at a gross bit rate of 1.152 Mbps. Each frame is divided into two halves of twelve contiguous slots, one half each for the uplink and downlink directions. Each full slot is of 480 bits, with a 32-bit S field for synchronization, 64-bit A field for signaling, and 328-bit B field for data and error control bits. The remaining bits are guard bits to account for propagation delay between the portable part (PP) and the radio fixed part (RFP), and to allow time for frequency switching and power ramping. The S-field consists of a 16-bit preamble of alternating 1s and 0s, followed by a fixed 16-bit packet synchronization word. The frame and slot structures are shown in Figure 6. The modulation used is Gaussian Frequency Shift Keying (GFSK) with a bandwidth-bit period product of 0.5. A 2G radio module based on a simple non-coherent receiver is being used in most DECT systems, including corDECT [1].

![DECT Frame and Slot Structure](image)

Figure 6. DECT Frame and Slot Structure.